CLAIM AMENDMENTS:

A listing of the entire set of claims 1-25 is submitted herewith per 37 CFR §1.121. This listing of claims 1-25 will replace all prior versions, and listings, of claims in the application.

1. (Original) A method of plating an integrated circuit, comprising:

positioning an activation plate adjacent to at least one integrated circuit, the integrated circuit including a plurality of bond pads comprising a bond-pad metal, and the activation plate comprising the bond-pad metal;

plating a layer of electroless nickel on the bond pads and the activation plate; and

plating a layer of gold over the layer of electroless nickel on the bond pads and the activation plate.

2. (Original) The method of claim 1 wherein the bond-pad metal comprises copper.

3. (Original) The method of claim 1 wherein the bond-pad metal comprises aluminum.

4. (Original) The method of claim 1 wherein the activation plate is positioned a distance between 0.125 inches and 0.250 inches from the at least one integrated circuit.

5. (Original) The method of claim 1 wherein the layer of electroless nickel is plated to a thickness between 0.5 microns and 5.0 microns.

6. (Original) The method of claim 1 wherein the layer of gold is plated to a thickness between 0.05 microns and 1.5 microns.

7. (Original) The method of claim 1 wherein the layer of gold is plated using one of an immersion gold or an electroless gold.

8. (Original) The method of claim 1 wherein the at least one integrated circuit is contained on a semiconductor wafer.

9. (Original) The method of claim 1 wherein the at least one integrated circuit is mounted on a carrier substrate when the layer of electroless nickel is plated.

10. (Original) The method of claim 1 further comprising:

plating a layer of electroless palladium on the plurality of bond pads and the activation plate after plating the layer of electroless nickel and prior to plating the layer of gold.

11. (Original) The method of claim 10 wherein the layer of electroless palladium is plated to a thickness between 0.2 microns and 1.0 micron.

12. (Original) The method of claim 1 further comprising:

zincating the plurality of bond pads and the activation plate prior to plating the layer of electroless nickel, the bond-pad metal comprising aluminum.

13. (Original) A system for plating an integrated circuit, comprising:

means for positioning an activation plate adjacent to at least one integrated circuit, the integrated circuit including a plurality of bond pads comprising a bond-pad metal, and the activation plate comprising the bond-pad metal;

means for plating a layer of electroless nickel on the bond pads and the activation plate; and

means for plating a layer of gold over the layer of electroless nickel on the bond pads and the activation plate.

14. (Original) The system of claim 13 wherein the activation plate is positioned a distance between 0.125 inches and 0.250 inches from the at least one integrated circuit.

15. (Original) The system of claim 13 further comprising:

means for plating a layer of electroless palladium on the bond pads and the activation plate after plating the layer of electroless nickel and prior to plating the layer of gold.

16. (Original) The system of claim 13 further comprising:

means for zincating the plurality of bond pads and the activation plate prior to plating the layer of electroless nickel, the bond-pad metal comprising aluminum.

17.-25. (Cancelled)